## REMARKS

Claims 32 through 39 and 44 through 53 are currently pending in the application.

Claims 1 through 31 are directed to a non-elected invention.

Claims 40, 41, 42, 43, 54, and 55 have been canceled.

Claims 32 through 39 and 44 through 53 currently stand rejected.

This amendment is in response to the Final Office Action of April 19, 2002.

Applicants submit herewith, under cover of a separate letter, a Letter to the Chief Draftsman for proposed corrections to FIGS. 9 and 10 of the drawings. All proposed corrections have been marked in red. Applicants respectfully request approval of the corrections to the drawings and will file corrected formal drawings upon receipt of such approval and a Notice of Allowance and Issue Fee Due in the application.

Claim 32 was objected to due to informalities in the claim language. Appropriate correction has been made.

Claims 32 through 37, 39, 44 through 49 and 51 through 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (U.S. Patent 5,998,860) in view of Akram et al. (U.S. Patent 5,811,879) and Swamy et al. (U.S. Patent 5,835,357).

Claims 32, 38, 44, 50, 52 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu (U.S. Patent 5,243,497) in view of Swamy et al.

Claims 35 through 37, 39, 47 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Swamy et al., as applied to claims 32 and 44 above, and further in view of Chan et al.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants submit that the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention. More specifically, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness because the cited prior art contains no suggestion therein for any combination thereof and is directed to diverse processes and equipment not readily capable of modification, there has not been and can be no showing of success for any combination of the cited prior art, any combination of the cited prior art fails to teach or suggest all the claim limitations of the present invention, and any rejection of the present invention based upon the cited prior art would be a hindsight reconstruction of the presently claimed invention by picking and choosing among the elements of the cited prior art based solely upon Applicants' disclosure.

Claims 32 through 37, 39, 44 through 49, and 51 through 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (U.S. Patent 5,998,860) in view of Akram et al. (U.S. Patent 5,811,879) and Swamy et al. (U.S. Patent 5,835,357). Applicants submit that a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established with respect to claims 32 through 37, 39, 44 through 49 and 53 because each and every element of the claims are not taught or suggested by the cited prior art references. Furthermore, Applicants submit that there is no suggestion or motivation to combine or modify the cited references as suggested in the Office Action.

Turning now to independent claim 32, Chan does not disclose connecting the conductor patterns on each side of the substrate with vias or forming an input/output connector comprising a ball-grid-array as stated in the Office Action. (*See*, Office Action, pages 4 and 5). Applicants submit that Akram does not disclose forming a pattern of electrical conductors on the first side

and the second side of the substrate. As disclosed in Akram, electrical conductors are formed on only one side of the substrate, therefore conductive vias are not used to connect electrical conductors on the first side and second side of the substrate. Thus, Applicants submit that it would not have been obvious to use the conductive vias disclosed in Akram to connect the conductor patterns on each side of the substrate of Chan. Also, because electrical conductors are formed on only one (the first) side of the substrate in Akram, Akram does not disclose attaching the active surface of semiconductor die to the second side of the substrate with vias. (*See*, U.S. Patent 5,811,879, FIG. 3 and accompanying text). Therefore, each and every element of independent claim 32 is not taught or suggested by Chan or Akram, alone or in any combination, and Applicants submit that a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established with respect to independent claim 32.

Since neither Chan nor Akram, alone or in combination, teach or suggest each and every limitation of independent claim 32, there must be a motivation or suggestion to modify and combine the cited prior art references. The Office Action alleges that "it would have been obvious to one of ordinary skill in the art to form the inherent internal circuitry of conductive vias, because, in the absence of the disclosure of any particular interconnection method, one of ordinary skill in the art would look to use a conventional process, such as that of Akram, to form the required circuitry." (Office Action, page 5).

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916. F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). The Office Action states "[i]n order for the dice on both sides of the package to be electrically connected to one another, there must be connections present in the form of internal circuitry within the circuit board, as is conventional in the art." (Office Action, page 4). The Office Action does not indicate where a motivation or suggestion exists in Chan or Akram to electrically connect dice on both sides of the package as alleged in the Office Action. Further, Applicants contend that there is no suggestion or motivation in Chan to use a ball-grid array as an input/output connector, and that it would not

have been obvious to modify Chan in view of Akram or Swamy without a suggestion or motivation to do so. Therefore, since the Examiner has not indicated where a suggestion or a motivation exists to combine or modify the prior art references, Applicants submit that the Office has not met the burden of establishing a *prima facie* case of obviousness under 35 U.S.C. § 103, but is rather relying on a hindsight reconstruction using the Applicants' disclosure to formulate the obviousness rejection.

Turning now to independent claim 44, Applicants have amended the claim to include the limitations of forming electrical conductors on each of the first and second sides of the substrate, and connecting the electrical conductors on the first and second sides with conductive vias. As previously discussed herein, Chan does not disclose connecting the conductor patterns on each side of the substrate with vias or forming an input/output connector comprising a ball-grid-array. Furthermore, Akram does not disclose forming a pattern of electrical conductors on the first side and the second side substrate, using conductive vias are to connect electrical conductors on the first side and second side of the substrate, or attaching the active surface of semiconductor die to the second side of the substrate as previously discussed herein. Accordingly, Applicants submit that a *prima facie* case of obviousness has also not been established with respect to independent claim 44 since each and every element and claim 44 is not taught or suggested by Chan or Akram, alone or in ANY combination. Further, Applicants contend that since there is no suggestion or motivation to combine the cited references, the Office is using a hindsight reconstruction based on the Applicants' disclosure.

With regard to dependent claims 33 through 37, 39, 45 through 49 and 51, Applicants submit they are allowable at the very least as depending from non-obvious independent claims 32 or 44. If an independent claim is nonobvious, then any claim dependent from the independent claim is nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, Applicants request reconsideration and withdrawal of the obviousness rejections of claims 32 through 37, 39, 44 through 49, and 51.

Claims 32, 38, 44, 50, 52 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu (U.S. Patent 5,243,497) in view of Swamy et al. Applicants contend that a *prima facie* case of obviousness UNDER 35 U.S.C. § 103has not been established with respect to claims 32, 38, 44, and 50 because each and every element of the claims is not taught or suggested by the cited prior art references. Further, Applicants submit that there is no suggestion or motivation to combine or modify the cited prior art references as suggested in the Office Action.

With regard to the Chiu reference, and as stated in the Office Action Chiu "does not specifically disclose forming a circuitry pattern on both the first and second sides of the board," "does not disclose the circuit board (substrate) to have an input/output connector," "does not disclose connecting the conductor patterns with vias through the substrate," and "does not disclose an input/output connector connected to the package." (Office Action, pages 6-8). Therefore, each and every element of the claims are not taught or suggested by the cited prior art references, and Applicants submit that the Office has not established a *prima facie* case of obviousness under 35 U.S.C. § 103.

In rejecting the Applicants' claims, the Office relies on allegedly inherent features of the Chiu reference. The Office Action states that Chiu "inherently requires a pattern of circuitry to be on both sides on the board," "must inherently have an input/output connector so that the semiconductor dice can be electrically accessed by the hardware that it is connected to," "[the inherently present input/output connector] must also inherently be connected to the terminal contacts (34) in order to be electrically connected to the dice," "must be connections present in the form of internal circuitry [vias] within the circuit board, as is conventional in the art," and "an integrated circuit package must inherently have some form of an input/output connector." (*Id.*).

"The mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency.]" *In re Rijckaert*, 9 F. 3d 1531, 1534, 28 USPQ2d 1955 (Fed. Cir. 1993), *quoting In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "That which may be inherent is not necessarily known. Obviousness cannot be predicated on

what is unknown." *Id. quoting In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966). "Such a retrospective view of inherency is not a substitute for some teaching or suggestion supporting an obviousness rejection." *Id.* Applicants contend that the Office has not indicated where the inherent teachings or suggestions appear in the prior art and assert that the obviousness rejections based on inherent features are reconstructed using the teachings of the Applicants' disclosure to formulate the obviousness rejections. Further, Applicants contend that it would not have been obvious to use conductive vias of Swamy to electrically connect the circuitry on the first and second sides of the board, because Chiu does not disclose forming circuitry on both the first and second sides of the board.

Since Chiu does not teach each and every aspect of independent claims 32 or 44 as stated in the Office Action, and since the Office has not indicated where the cited prior art references suggest or motivate modifying the teachings of the prior art, Applicants submit that a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established with regard to claims 32 and 44. Since claims 38 and 50 depend from non-obvious independent claims, they are also non-obvious. Accordingly, Applicants request the reconsideration and withdrawal of the obviousness rejections of claims 32, 38, 44, and 50.

Applicants submit that claims 32 through 39 and 44 through 51 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 32 through 39 and 44 through 51 and the case passed for issue.

Applicants request the entry of this amendment for the following reasons:

The amendment is timely filed.

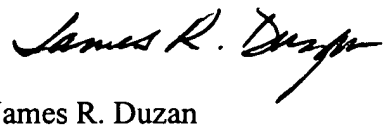
The amendment clearly places the application in condition for allowance.

The amendment does not require any further search or consideration by the Examiner.

The amendment reduces or simplifies the number of issues for any subsequent appeal.

In summary, Applicants request entry of this amendment, allowance of the presently pending claims, and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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**APPENDIX A**

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:



32. (Three Times Amended) A method for forming a high density multi-chip module, comprising:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die of said plurality having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;

forming a pattern of a plurality of electrical conductors associated with said substrate [one each] on each of said first side and second side of said substrate, at least one electrical conductor of said plurality of electrical conductors having a connection terminal adjacent a through-slot of said at least three through-slots for connecting said plurality of bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

connecting said conductor pattern on said first side and said second side of said substrate with conductive vias through said substrate;

forming an input/output connector on said substrate and connecting said input/output connector to said plurality of electrical conductors, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said plurality of semiconductor dice;

attaching the active surfaces of a plurality of said plurality of semiconductor dice to the first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the plurality of bond pads of said at least one semiconductor die aligned with other alternate through-slots of said at least three through-slots for access from the first side of said substrate; and

wire-bonding said plurality of bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the alternate through-slots.

44. (Thrice Amended) A method for forming a high density multi-chip module, comprising:

providing a plurality of integrated circuit dice, each die of said plurality having an active surface with a row of conductive bond pads thereon;

forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;

forming a pattern of electrical conductors associated with said substrate <u>on each of said first and second sides of said substrate</u> and having connection terminals adjacent each of said at least three through-slots for connecting said bond pads to an input/output connector;

<u>connecting said conductor patterns on said first and second sides with conductive vias through said substrate;</u>

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said bond pads, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice;

attaching the active surfaces of a plurality of said plurality of integrated circuit dice to said first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one of said plurality of dice to said second side of said substrate wherein the bond pads thereof are aligned with other alternate through-slots for access from the first side of said substrate; and

wire-bonding said bond pads of each attached die to connection terminals adjacent the corresponding through-slot.